In The Claims:

The listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-2 (canceled).

3. (previously presented) The method according to Claim 6, wherein the substrate comprises an integrated circuit substrate, wherein the raised pattern comprises a pattern of transistor gate electrodes, and wherein maintaining portions of the first insulating layer on the substrate comprises maintaining portions of the first insulating layer between transistor gate electrodes.

Claims 4-5 (canceled).

6. (currently amended) A method of forming an electronic device including a substrate and a raised pattern on the substrate, the method comprising:

forming a first insulating layer on the raised pattern and on the substrate wherein forming the first insulating layer comprises forming a first portion of the first insulating layer using a first processing condition and forming a second portion of the first insulating layer using a second processing condition;

after forming the first insulating layer including the first and second portions, removing portions of the first insulating layer to expose portions of the raised pattern while maintaining portions of the first insulating layer on the substrate; and

after removing portions of the first insulating layer, forming a second insulating layer on the exposed portions of the raised pattern and on the maintained portions of the first insulating layer;

wherein the first insulating layer includes closed voids therein, and wherein removing portions of the first insulating layer comprises opening the voids in the first insulating layer, and

wherein openings in the voids are substantially at least as wide as any portions of the opened voids between the openings and the substrate;

wherein the substrate comprises an integrated circuit substrate, wherein the raised pattern comprises a pattern of memory array bit lines, and wherein maintaining portions of the first insulating layer on the substrate comprises maintaining portions of the first insulating layer between memory array bit lines.

7. (previously presented) The method according to Claim 6, wherein the closed voids are located in the first insulating layer between portions of the raised pattern.

8. (previously presented) The method according to Claim 6, wherein the second insulating layer fills the opened voids.

9. (currently amended) ~~The method according to Claim 6,~~ A method of forming an electronic device including a substrate and a raised pattern on the substrate, the method comprising:

forming a first insulating layer on the raised pattern and on the substrate wherein forming the first insulating layer comprises forming a first portion of the first insulating layer using a first processing condition and forming a second portion of the first insulating layer using a second processing condition;

after forming the first insulating layer including the first and second portions, removing portions of the first insulating layer to expose portions of the raised pattern while maintaining portions of the first insulating layer on the substrate; and

after removing portions of the first insulating layer, forming a second insulating layer on the exposed portions of the raised pattern and on the maintained portions of the first insulating layer;

wherein the first insulating layer includes closed voids therein, and wherein removing portions of the first insulating layer comprises opening the voids in the first insulating layer, and

wherein openings in the voids are substantially at least as wide as any portions of the opened voids between the openings and the substrate;

wherein ~~wherein:~~ forming the first portion of the first insulating layer using the first processing condition comprises forming the first portion of the first insulating layer using a first ~~pressure;~~ pressure, and forming the second portion of the first insulating layer using the second processing condition comprises forming the second portion of the first insulating layer using a second pressure different than the first pressure.

10. (currently amended) ~~The method according to Claim 6,~~ A method of forming an electronic device including a substrate and a raised pattern on the substrate, the method comprising:

forming a first insulating layer on the raised pattern and on the substrate wherein forming the first insulating layer comprises forming a first portion of the first insulating layer using a first processing condition and forming a second portion of the first insulating layer using a second processing condition;

after forming the first insulating layer including the first and second portions, removing portions of the first insulating layer to expose portions of the raised pattern while maintaining portions of the first insulating layer on the substrate; and

after removing portions of the first insulating layer, forming a second insulating layer on the exposed portions of the raised pattern and on the maintained portions of the first insulating layer;

wherein the first insulating layer includes closed voids therein, and wherein removing portions of the first insulating layer comprises opening the voids in the first insulating layer, and wherein openings in the voids are substantially at least as wide as any portions of the opened voids between the openings and the substrate

wherein ~~wherein:~~ forming the first portion of the first insulating layer using the first processing condition comprises forming the first portion of the first insulating layer using a first bias ~~power;~~ power, and forming the second portion of the first insulating layer using the second

processing condition comprises forming the second portion of the first insulating layer using a second bias power different than the first bias power.

11. (currently amended) ~~The method according to Claim 6,~~ A method of forming an electronic device including a substrate and a raised pattern on the substrate, the method comprising:

forming a first insulating layer on the raised pattern and on the substrate wherein forming the first insulating layer comprises forming a first portion of the first insulating layer using a first processing condition and forming a second portion of the first insulating layer using a second processing condition;

after forming the first insulating layer including the first and second portions, removing portions of the first insulating layer to expose portions of the raised pattern while maintaining portions of the first insulating layer on the substrate; and

after removing portions of the first insulating layer, forming a second insulating layer on the exposed portions of the raised pattern and on the maintained portions of the first insulating layer;

wherein the first insulating layer includes closed voids therein, and wherein removing portions of the first insulating layer comprises opening the voids in the first insulating layer, and wherein openings in the voids are substantially at least as wide as any portions of the opened voids between the openings and the substrate

wherein ~~wherein:~~ forming the first portion of the first insulating layer using the first processing condition comprises forming the first portion of the first insulating layer using a pressure in the range of about 1 milliTorr to about 5 milliTorr and a bias power in the range of about 500 Watts to about 1500 Watts.

12. (original) The method according to Claim 11, wherein forming the first portion of the first insulating layer using the first processing condition comprises using a processing gas including an oxygen gas at a flow rate in the range of about 30sccm to about 150sccm, a helium

gas at a flow rate in the range of about 10sccm to about 200sccm, and a silane gas at a flow rate in the range of about 10sccm to about 100sccm.

13. (previously presented) The method according to Claim 6, wherein:

forming the second portion of the first insulating layer using the second processing condition comprises forming the second portion of the first insulating layer using a pressure in the range of about 3 milliTorr to about 10 milliTorr and a bias power in the range of about 1000 Watts to about 5000 Watts.

14. (original) The method according to Claim 13, wherein forming the second portion of the first insulating layer using the second processing condition comprises using a processing gas including an oxygen gas at a flow rate in the range of about 30sccm to about 150sccm, a helium gas at a flow rate in the range of about 10sccm to about 300sccm, and a silane gas at a flow rate in the range of about 10sccm to about 100sccm.

15. (previously presented) The method according to Claim 6, wherein forming the first insulating layer comprises forming the first insulating layer using a high density plasma chemical vapor deposition (HDP-CVD).

Claim 16 (canceled).

17. (currently amended) ~~The method according to Claim 16,~~ A method of forming an electronic device including a substrate and a raised pattern on the substrate, the method comprising:

forming a first insulating layer on the raised pattern and on the substrate wherein forming the first insulating layer comprises forming a first portion of the first insulating layer using a first processing condition and forming a second portion of the first insulating layer using a second processing condition;

after forming the first insulating layer including the first and second portions, removing portions of the first insulating layer to expose portions of the raised pattern while maintaining portions of the first insulating layer on the substrate; and

after removing portions of the first insulating layer, forming a second insulating layer on the exposed portions of the raised pattern and on the maintained portions of the first insulating layer;

wherein the first insulating layer includes closed voids therein, and wherein removing portions of the first insulating layer comprises opening the voids in the first insulating layer, and wherein openings in the voids are substantially at least as wide as any portions of the opened voids between the openings and the substrate;

wherein removing portions of the first insulating layer comprises etching back portions of the first insulating layer without mechanical polishing while etching back;

wherein removing portions of the first insulating layer further comprises mechanical polishing separate from etching back.

18. (previously presented) The method according to Claim 6, wherein removing portions of the first insulating layer comprises removing portions of the first insulating layer beyond portions of the raised pattern so that the raised pattern extends beyond the maintained portions of the first insulating layer and so that the maintained portions of the first insulating layer are recessed relative to the exposed portions of the raised pattern.

19. (previously presented) The method according to Claim 6, wherein a height of the first insulating layer between portions of the raised pattern is greater than a height of the raised pattern before removing portions of the first insulating layer.

Claims 20-21 (canceled).

22. (previously presented) The method according to Claim 25, wherein removing portions of the first insulating layer comprises etching back portions of the first insulating layer without mechanical polishing while etching back.

23. (currently amended) ~~The method according to Claim 25,~~ A method of forming an electronic device including a substrate and a raised pattern on the substrate, the method comprising:

forming a first insulating layer on the raised pattern and on the substrate wherein a height of the first insulating layer between portions of the raised pattern is greater than a height of the raised pattern;

after forming the first insulating layer, removing portions of the first insulating layer while maintaining portions of the first insulating layer so that the raised pattern extends beyond the maintained portions of the first insulating layer and so that the maintained portions of the first insulating layer are recessed between portions of the raised pattern; and

after removing portions of the first insulating layer, forming a second insulating layer on exposed portions of the raised pattern and on the maintained portions of the first insulating layer;

wherein the first insulating layer includes closed voids therein, and wherein removing portions of the first insulating layer comprises opening the voids in the first insulating layer wherein openings in the voids are substantially at least as wide as portions of the opened voids between the openings and the substrate;

wherein removing portions of the first insulating layer further comprises mechanical polishing separate from etching back.

Claim 24 (canceled).

25. (currently amended) A method of forming an electronic device including a substrate and a raised pattern on the substrate, the method comprising:

forming a first insulating layer on the raised pattern and on the substrate wherein a height of the first insulating layer between portions of the raised pattern is greater than a height of the raised pattern;

after forming the first insulating layer, removing portions of the first insulating layer while maintaining portions of the first insulating layer so that the raised pattern extends beyond the maintained portions of the first insulating layer and so that the maintained portions of the first insulating layer are recessed between portions of the raised pattern; and

after removing portions of the first insulating layer, forming a second insulating layer on exposed portions of the raised pattern and on the maintained portions of the first insulating layer;

wherein the first insulating layer includes closed voids therein, and wherein removing portions of the first insulating layer comprises opening the voids in the first insulating layer wherein openings in the voids are substantially at least as wide as portions of the opened voids between the openings and the substrate;

wherein forming the first insulating layer comprises forming a first portion of the first insulating layer using a first processing condition including a first pressure and a first bias power and forming a second portion of the first insulating layer using a second processing condition including a second pressure different than the first pressure and a second bias power different than the first bias power.

26. (previously presented) The method according to Claim 25, wherein the closed voids are located in the first insulating layer between portions of the raised pattern.

27. (original) The method according to Claim 26, wherein the second insulating layer fills the opened voids.

Claims 28-75 (canceled).